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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,007	WHEELER ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment file September 12, 2005. Claims 1 – 29 have been examined. Claims 1 – 29 have been rejected.

Response to Remarks

2. Regarding claim rejections under 35 USC § 102, **claims 1 and 13**:

2.1. The Applicant argues specifically that:

2.1.1. On page 3 of the Remarks, third paragraph, the state table 318 in Watkins is representative of logic design verification and does not represent instrumentation data such as the utilization statistics of the logic design elements. Also, state table 318 is populated by iterative invocations of the simulator and the data in the table is not collected automatically.

2.1.1.1. The Examiner respectfully replies, that the state table 318 in Watkins is representative of data for logic design verification, which under the broadest reasonable interpretation is instrumentation data. The state table is populated by iterative invocations of the simulator, but this has no bearing on whether the data is automatically collected. The user designates the points to be monitored during simulation (Watkins, column 5, lines 5 – 10), and the data from the monitoring points are automatically collected.

2.1.2. On page 4 of the Remarks, first paragraph, Watkins does not disclose automatically collecting instrumentation data relating to the logic design element during the simulation. The instrumentation data may represent, for example, utilization statistics that may provide insight into system architecture.

2.1.2.1. The Examiner respectfully replies that the user designates the points to be monitored during simulation (Watkins, column 5, lines 5 – 10), and the data from the monitoring points are automatically collected. In response to applicant's argument that the references fail to show that the instrumentation data may represent, for example, utilization statistics, it is noted that the features upon which applicant relies (i.e., that the instrumentation data may represent, for example, utilization statistics) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

2.2. Accordingly, as discussed above, the rejections are maintained.

3. Regarding claim rejections under 35 USC § 102, **claims 2 - 6 and 14 - 18**:

3.1. The Applicant argues that the claims are allowable because they depend from claims 1 and 13. The Examiner respectfully replies that the rejections of claims 1 and 13 were maintained. Accordingly, the rejections of claims 2 - 6 and 14 – 18 are maintained.

4. Regarding claim rejections under 35 USC § 102, **claim 25**:

4.1. The Applicant argues specifically that:

4.1.1. On page 5 of the Remarks, first paragraph, Watkins is silent on a logic design element arranged to automatically collect instrumentation data relating to the logic design element during the simulation as required by claim 25.

4.1.1.1. The Examiner replies that the limitations are taught in Watkins as follows:

4.1.1.1.1. Watkins appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

4.1.1.1.1.1. Regarding (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***); figure 2, element 224, is a simulation module.

4.1.1.1.2. Watkins appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect instrumentation data relating to the logic design element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***).

4.1.1.1.2.1. Regarding (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***); Watkins teaches software that collects data, therefore it would have been inherent that the software has a portion of code to collect data, which is a collection module.

4.2. Accordingly, the rejection is maintained.

5. Regarding claim rejections under 35 USC § 102, **claims 26 - 27**:

5.1. The Applicant argues that the claims are allowable because they depend from claim 25. The Examiner respectfully replies that the rejection of claim 25 was maintained. Accordingly, the rejections of claims 26 - 27 are maintained.

6. Regarding claim rejections under 35 USC § 103 (Watkins/Sharma), **claims 7 and 19**:

6.1. The Applicant argues that:

6.1.1. On page 6 of the Remarks, paragraph 2, Watkins does not teach a logic design element that can automatically collect the instrumentation data during simulation.

6.1.1.1. The Examiner respectfully replies that Watkins teaches a logic design element that can automatically collect the instrumentation data during simulation at ***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***. Especially in reference to figure 3 and column 10, lines 64 – 68, the state table 318 contains monitored nodes and simulation data collected during simulation. The data is collected automatically during simulation for a logic design element.

6.1.2. On page 6 of the Remarks, paragraph 2, Sharma is silent on using a FIFO to automatically collect instrumentation data corresponding to the FIFO during simulation.

6.1.2.1. The Examiner respectfully replies that it would have been obvious to an ordinary artisan at the time of invention to use the FIFO logic element of Sharma with the art of Watkins (described above) to produce a FIFO logic element to automatically collect instrumentation data corresponding to the FIFO during simulation.

6.1.3. On page 6 of the Remarks, paragraph 3, Watkins and Sharma, together or individually, do not teach all the limitations of claims 7 and 19. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Sharma with the art of Watkins to come up with the invention covered by the scope of claims 7 and 19.

6.1.3.1. The Examiner respectfully replies that, as discussed above, Watkins and Sharma, together, teach all the limitations of claims 7 and 19. Since the premise is of the argument is rebutted, the conclusion does not stand.

6.2. Accordingly, the rejections of claims 7 and 19 are maintained.

7. Regarding claim rejections under 35 USC § 103 (Watkins/Sharma), **claims 8 - 9 and 20 - 21**:

7.1. The Applicant argues that the claims are allowable because they depend from one of claims 7 and 19. The Examiner respectfully replies that the rejection of claims 7 and 19 was maintained. Accordingly, the rejections of claims 8 - 9 and 20 - 21 are maintained.

8. Regarding claim rejection under 35 USC § 103 (Watkins/Sharma), **claim 28**:

8.1. The Applicant argues that:

8.1.1. The claim is allowable because it depends from claim 25.

8.1.1.1. The Examiner respectfully replies that the rejection of claim 25 was maintained. Accordingly, the rejection of claim 28 is maintained.

8.1.2. Watkins and Sharma do not teach every limitation of claim 28.

8.1.2.1. The Examiner replies that claim 28 is taught by Watkins and Sharma as discussed below:

8.1.2.1.1. Watkins teaches that the collection module is integrated with the logic design element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

8.1.2.1.2. Watkins does not specifically teach that the collection module is integrated with the ***FIFO memory*** and is structured and arranged to automatically collect the instrumentation data relating to the ***FIFO memory*** during the simulation.

8.1.2.1.3. Sharma teaches that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

8.1.3. Watkins and Sharma, together or individually, do not teach all the limitations of claim 28. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Sharma with the art of Watkins to come up with the invention covered by the scope of claim 28.

8.1.3.1. The Examiner respectfully replies that, as discussed above, Watkins and Sharma, together, teach all the limitations of claim 28. Since the premise is of the argument is rebutted, the conclusion does not stand.

8.2. Accordingly, the rejection of claim 28 is maintained.

9. Regarding claim rejection under 35 USC § 103 (Watkins/Mitchell), **claims 10 and 22**:

9.1. The Applicant argues that:

9.1.1. On page 8 of the Remarks, paragraph 2, Watkins is silent on automatically collecting instrumentation data of a logic design element during simulation (in column 7, lines 12 – 17 of Watkins).

9.1.1.1. The Examiner respectfully replies that in column 7, lines 12 – 17 of Watkins, Watkins teaches that the simulator performs a simulation run and places the simulation results into a data structure, which is displayed on the screen. The

data is instrumentation data, which is collected automatically during the simulation run.

9.1.2. On page 8 of the Remarks, paragraph 2, Mitchell is silent on automatically collecting instrumentation data of a logic design element during simulation.

9.1.2.1. The Examiner respectfully replies that Watkins teaches the limitation, as discussed above.

9.1.3. Watkins and Mitchell, together or individually, do not teach all the limitations of claims 10 and 22. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Mitchell with the art of Watkins to come up with the invention covered by the scope of claims 10 and 22.

9.1.3.1. The Examiner respectfully replies that, as discussed above, Watkins and Mitchell, together, teach all the limitations of claims 10 and 22. Since the premise is of the argument is rebutted, the conclusion does not stand.

10. Regarding claim rejections under 35 USC § 103, **claims 11 – 12 and 23 - 24**:

10.1. The Applicant argues that the claims are allowable because they depend from one of claims 10 and 22. The Examiner respectfully replies that the rejections of claims 10 and 22 were maintained. Accordingly, the rejections of claims 11 – 12 and 23 – 24 are maintained.

11. Regarding claim rejection under 35 USC § 103, **claim 29**:

11.1. The Applicant argues that:

11.1.1. The claim is allowable because it depends from claim 25.

11.1.1.1. The Examiner respectfully replies that the rejection of claim 25 was maintained. Accordingly, the rejection of claim 29 is maintained.

11.1.2. Watkins and Mitchell do not teach every limitation of claim 29.

11.1.2.1. The Examiner replies that claim 29 is taught by Watkins and Mitchell as discussed below:

11.1.2.1.1. Watkins appears to teach that the collection module is integrated with the logic element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***column 7, lines 12 – 17***).

11.1.2.1.2. Mitchell appears to teach that a logic design element includes a tri-state bus (***Abstract, and figure 1***).

11.1.2.1.3. It would have been obvious to an ordinary artisan at the time of invention to use the art of Watkins with the art of Mitchell to produce the claimed invention.

11.1.3. Watkins and Mitchell, together or individually, do not teach all the limitations of claim 29. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Sharma with the art of Watkins to come up with the invention covered by the scope of claim 29.

11.1.3.1. The Examiner respectfully replies that, as discussed above, Watkins and Mitchell, together, teach all the limitations of claim 29. Since the premise is of the argument is rebutted, the conclusion does not stand.

11.2. Accordingly, the rejection of claim 29 is maintained.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1 – 6 and 13 - 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

13.1. Regarding claims 1 and 13:

13.1.1. Watkins appears to teach a method and machine-accessible medium using a logic design element in a logic design (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

13.1.2. Watkins appears to teach a method and machine-accessible medium performing a simulation of the logic design that includes simulating the logic design element (***figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

13.1.3. Watkins appears to teach a method and machine-accessible medium having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 - 49***).

13.2. Regarding claims 2 and 14:

13.2.1. Watkins appears to teach displaying the instrumentation data relating to the logic design element (***Figure 3***).

13.3. Regarding claims 3 and 15:

13.3.1. Watkins appears to teach receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

13.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

13.4. Regarding claims 4 and 16:

13.4.1. Watkins appears to teach displaying the instrumentation data after performing the simulation (***column 5, lines 14 – 16***).

13.5. Regarding claims 5 and 17:

13.5.1. Watkins appears to teach displaying the instrumentation data while performing the simulation (***column 7, lines 48 – 57***).

13.6. Regarding claims 6 and 18:

13.6.1. Watkins appears to teach performing the simulation means performing a partial simulation (***column 7, lines 12 – 27***).

13.6.2. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the partial simulation (***column 7, lines 24 – 27***).

13.6.3. Watkins appears to teach displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation (***column 7, lines 12 – 27***).

14. Claims 25 -27 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,220,512).

14.1. Regarding claim 25:

14.1.1. Watkins appears to teach a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***).

14.1.1.1. Regarding (***figure 2, element 224; figure 4; and column 8, lines 4 – 6; and column 1, lines 15 - 49***); figure 2, element 224, is a simulation module.

14.1.2. Watkins appears to teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect instrumentation data relating to the logic design element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***).

14.1.2.1. Regarding (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 – 4; and column 1, lines 15 – 49; and column 7, lines 12 - 27***); Watkins teaches software that collects data, therefore it would have been inherent that the software has a portion of code to collect data, which is a collection module.

14.2. Regarding claim 26:

14.2.1. Watkins appears to teach a display module that is structured and arranged to display the instrumentation data relating to the logic element design (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***).

14.2.1.1. Regarding (***column 7, lines 12 – 19; and figure 3; and figure 2, element 224***); Column 7, lines 12 – 19, recites that the simulation module displays the instrumentation data; therefore the logic simulator (***figure 2, element 224***) is a display module.

14.3. Regarding claim 27:

14.3.1. Watkins appears to teach an interface module that is structured and arranged to receive a query to display the instrumentation data relating to the design element, wherein the display module is structured and arranged to display the instrumentation data relating to the logic design element in response to the query (***column 6, lines 45 – 53***).

14.3.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query. Watkins teaches software to receive a query, therefore it is inherent that there is a portion of code that receives the query, which is an interface module to receive the query.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. xClaims 7 – 9 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Sharma (U.S. Patent 5,978,574).

17.1. Claim 7 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

17.2. Claim 19 is a dependent claim of claim 13, and thereby inherits all of the rejected limitations of claim 13.

17.3. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

17.4. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

17.5. Regarding claims 7 and 19:

17.5.1. Watkins appears to teach having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the logic element (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

17.5.2. Watkins does not specifically teach that ***the logic design element includes a FIFO memory***, and having the logic design element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***FIFO memory***.

17.5.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

17.5.4. The motivation to use the art of Sharma with the art of Watkins is the statement recited in Sharma that verification of queue flow control is traditionally performed through simulation (***column 2, lines 10 – 14; and column 2, lines 31 – 36***).

17.6. Regarding claims 8 and 20:

17.6.1. Watkins appears to teach having the logic elements record usage during the simulation (***figure 4; and column 5, lines 5 – 10; and column 6, lines 45 – 52; and column 7, lines 32 – 35***).

17.6.2. Watkins does not specifically teach having the ***FIFO memory*** record usage ***of the FIFO memory*** during the simulation.

17.6.3. Sharma appears to teach a FIFO memory simulation (***figure 2; and column 2, lines 10 – 13; and column 1, lines 31 – 35***).

17.7. Regarding claims 9 and 21:

17.7.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

17.7.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

17.7.2. Watkins appears to teach displaying the instrumentation data relating to the logic element in response to the query (***column 7, lines 36 - 45***).

17.7.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***FIFO memory***.

17.7.4. Watkins does not specifically teach displaying the instrumentation data relating to ***the FIFO memory*** in response to the query.

17.7.5. Sharma appears to teach a FIFO memory (***figure 2; and column 1, lines 63 - 67***).

17.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Sharma with the art of Watkins to produce the claimed invention.

18. Claims 10 - 12 and 22 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Mitchell (U.S. Patent 5,646,553).

18.1. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

18.2. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

18.3. Regarding claims 10 and 22:

18.3.1. Watkins appears to teach that having the logic element automatically collect the instrumentation data includes having the logic element automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the logic element (***column 7, lines 12 - 17***).

18.3.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

18.3.3. Watkins does not specifically teach having the logic element automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect the instrumentation data during the simulation, with the instrumentation data relating to the ***tri-state bus***.

18.3.4. Mitchell appears to teach that a logic design includes a tri-state bus (***Abstract, and figure 1***).

18.3.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 – 50***).

18.4. Regarding claims 11 and 23:

18.4.1. Watkins appears to teach that having a logic element automatically collect the instrumentation data includes having a logic element automatically collect usage of a logic element during the simulation (***column 7, lines 11 – 26; column 6, lines 45 – 53***).

18.4.2. Watkins does not specifically teach that having the ***tri-state bus*** automatically collect the instrumentation data includes having the ***tri-state bus*** automatically collect usage of the ***tri-state bus*** during the simulation.

18.4.3. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

18.5. Regarding claims 12 and 24:

18.5.1. Watkins appears to teach receiving a query to display the instrumentation data relating to a logic element (***column 6, lines 45 – 53***).

18.5.1.1. Regarding (***column 6, lines 45 – 53***); attaching a data area that displays state data is a query.

18.5.2. Watkins appears to teach displaying the instrumentation data relating to a logic element in response to the query (***column 7, lines 36 – 45***).

18.5.3. Watkins does not specifically teach receiving a query to display the instrumentation data relating to the ***tri-state bus***.

18.5.4. Watkins does not specifically teach displaying the instrumentation data relating to the ***tri-state bus*** in response to the query.

18.5.5. Mitchell appears to teach a logic design that includes a tri-state bus (***Abstract, and figure 1***).

19. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Sharma (U.S. Patent 5,978,574).

19.1. Claim 28 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

19.2. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

19.3. The art of Sharma is directed to verification of queue flow control through model checking (***Title***).

19.4. Regarding claim 28:

19.4.1. Watkins appears to teach that the collection module is integrated with the logic design element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***figure 3; and column 5, lines 5 – 10, especially "points to be monitored"; and column 10, lines 53 – 68; and column 11, lines 1 - 4***).

19.4.2. Watkins does not specifically teach that the collection module is integrated with the ***FIFO memory*** and is structured and arranged to automatically collect the instrumentation data relating to the ***FIFO memory*** during the simulation.

19.4.3. Sharma appears to teach that the logic design element includes a FIFO memory (***figure 2; and column 1, lines 63 – 67***).

19.4.4. The motivation to use the art of Sharma with the art of Watkins is the statement recited in Sharma that verification of queue flow control is traditionally performed through simulation (***column 2, lines 10 – 14; and column 2, lines 31 – 36***).

20. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,220,512) in view of Mitchell (U.S. Patent 5,646,553).

20.1. Claim 29 is a dependent claim of claim 25, and thereby inherits all of the rejected limitations of claim 25.

20.2. The art of Watkins is directed toward a system for simultaneous interactive presentation of electronic circuit diagrams and simulation data (***Title***).

20.3. The art of Mitchell is directed toward a driver for a tri-state bus (***Title***).

20.4. Regarding claim 29:

20.4.1. Watkins appears to teach that the collection module is integrated with the logic element and is structured and arranged to automatically collect the instrumentation data relating to the logic element during the simulation (***column 7, lines 12 - 17***).

20.4.2. Watkins does not specifically teach that ***the logic design element includes a tri-state bus***.

20.4.3. Watkins does not specifically teach that the collection module is integrated with the ***tri-state bus*** and is structured and arranged to automatically collect the instrumentation data relating to the ***tri-state bus*** during the simulation.

20.4.4. Mitchell appears to teach that a logic design element includes a tri-state bus (***Abstract, and figure 1***).

20.4.5. The motivation to use the art of Mitchell with the art of Watkins is the benefit recited in Mitchell that the circuit avoids contention on the bus by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device begins to drive, while holding the data on the bus until the end of the transfer cycle (***column 1, lines 45 - 50***).

Conclusion

21. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened

statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-262-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 11/2/05

Primary Examiner
Art Unit 2125